Citadel: Efficiently Protecting Stacked Memory From Large Granularity Failures

Dec 15th 2014
MICRO-47 Cambridge UK

Prashant Nair - Georgia Tech
David Roberts - AMD Research
Moinuddin Qureshi - Georgia Tech
INTRODUCTION TO 3D DRAM

• DRAM systems face a bandwidth wall

• Stack DRAM Dies over each other → 3D DRAM

• Use Through Silicon Vias (TSV) to connect Dies

• Higher density of TSV → Higher Bandwidth

Go 3D to Scale Bandwidth Wall

Courtesy MICRON, Extremetech
FAILURES IN 3D DRAM

• 3D DRAM → Communicate using TSVs

• A New Failure Mode: TSV Failures

• TSV Failures → Large Granularity Failures

TSVs Present New Kind of Large Granularity Failures
A NEW FAILURE MODE FROM TSVs

TSVs conduit for Address and Data

- Mainly Two Types TSV Faults
  - Data (Incorrect Data fetched from DRAM Die)
  - Address (Incorrect address presented to DRAM Die)

TSV Faults cause unavailability of Data and Addresses
EFFECT OF TSV FAULTS

• Data TSV Fault → Few Columns Faulty

• Address TSV Fault → 50% Memory Loss

TSVs can cause failures at multiple granularities
IMPACT OF TSV FAULTS

System: 8GB Stacked Memory (HBM)
Prob. System Failure $\rightarrow$ Prob(Uncorrectable Error)

Efficient Techniques to Mitigate TSV Faults
OTHER FAILURES STILL PRESENT

- Bit
- Word
- Column
- Row
- Bank

Apart from TSV Faults, 3D DRAM will also continue to have other multi-granularity failures
### 3D DRAM: FAILURE RATE

<table>
<thead>
<tr>
<th>Die Failure Mode</th>
<th><em>Permanent Fault Rate (FIT)</em></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>148.8</td>
</tr>
<tr>
<td>Word</td>
<td>2.4</td>
</tr>
<tr>
<td>Column</td>
<td>10.5</td>
</tr>
<tr>
<td>Row</td>
<td>32.8</td>
</tr>
<tr>
<td>Bank</td>
<td>80</td>
</tr>
</tbody>
</table>

- ✔ SECDED
- ✗ SECDED

1. Large Granularity Faults are as likely as Bit Faults
2. Low Cost Solutions Required For Large Faults

*Projected from Sridharan et. al. : DRAM Field Study*
Current Systems Naturally Stripe Data Across Chips

- **ChipKill**: Mitigate Large Failures (Whole Chip)

ChipKill relies on data striping to tolerate large granularity failures.
CHIPKILL IN STACKED MEMORY

- A request activates at least 8 Banks or 8 Channels

At least 8X↑ activation power, 8X↓ DRAM parallelism
Striping data across banks/channels in 3D is costly.
GOAL

Develop Efficient Solutions to Mitigate TSV and other Large Granularity Faults in Stacked Memory without striping data
• Introduction and Background

• Citadel

• Scheme - 1 : TSV-SWAP

• Scheme - 2 : Three Dimensional Parity (3DP)

• Scheme - 3 : Dynamic Dual Grain Sparing (DDS)

• Summary
CITADEL: AN OVERVIEW

- Runtime TSV Sparing (TSV-SWAP)
- RAID-5 across 3 dimensions (Tri dimensional parity)
- Spare Faults Regions (Dual Granularity Sparing)

Enable robust stacked memory at very low overheads
• Introduction and Background

• Citadel

• Scheme - 1 : TSV-SWAP

• Scheme - 2 : Three Dimensional Parity (3DP)

• Scheme - 3 : Dynamic Dual Grain Sparing (DDS)

• Summary
DESIGN-TIME TSV SPARING

Designers provision spares TSVs alongside Data TSVs and Address TSVs.

Additional Spare TSVs can replace faulty TSVs.
Deactivation of Faulty TSVs and Activation of Spare TSVs is performed at design time

• Deactivate Broken TSVs
• Activate SPARE TSVs
Additional TSVs are required for TSV Sparing and what happens if TSVs turn faulty at runtime?
TSV-SWAP: RUNTIME TSV SPARING

STEP-1: CREATE STANDBY TSVs

- Few Data TSVs as Standby TSVs
- Replicate Standby Data in ECC

Data TSVs reused as Standby TSVs
TSV-SWAP: RUNTIME TSV SPARING

STEP-2: DETECTING FAULTY TSVs

• CRC-32 address + data
• BIST diagnoses faulty TSVs

Data vs Address TSV Faults Using CRC-32+BIST
TSV-SWAP: RUNTIME TSV SPARING

STEP-3: REDIRECTING FAULTY TSVs

Swap Faulty TSVs with Standby TSVs at runtime

TSV-SWAP is a runtime technique that does not rely on additional spare TSVs
EFFECTIVENESS OF TSV-SWAP

Rate: One TSV Fault Every 7 years

Prob. Of System Failure

-1

-2

-3

With TSV Faults

TSV SWAP

No TSV Fault

Almost IDEAL

TSV-SWAP is Effective at Tolerating TSV Faults
• Introduction and Background

• Citadel

• Scheme - 1 : TSV-SWAP

• Scheme - 2 : Three Dimensional Parity (3DP)

• Scheme - 3 : Dynamic Dual Grain Sparing (DDS)

• Summary
TRI DIMENSIONAL PARITY (3DP)

- Use RAID-5 like scheme over three dimensions
- Detect using CRC-32
- Correct using Parity
  - Bank Level (BL) Parity
  - Row Level (RL-H) Parity per die
  - Row Level (RL-V) Parity across dies

Three Dimensions Help In Multi-Fault Handling
3DP: DATA CORRECTION

If Fault → Compute Parity and Correct

• 1-Small Fault → RL-H or RL-V
• 2-Small Faults → RL-H and RL-V
• 2 Small + 1 Large Fault → RL-H and RL-V and BL

Multiple Multi-granularity Faults Are Corrected At Runtime
OVERHEADS IN UPDATING PARITY

- RL-H and RL-V Parity just 32 KB stored in SRAM
- BL Parity is 128 MB stored in DRAM
- Updating BL Parity has performance overhead
- Employ Demand Caching of BL Parity in LLC
- Mitigate overheads of updating BL Parity

Demand Caching of BL Parity Has 85% Hit Rate And Mitigates Performance Overheads
EFFECTIVENESS OF 3DP

3DP is 7X Stronger Than A ChipKill-Like Scheme
• Introduction and Background
• Citadel
• Scheme - 1 : TSV-SWAP
• Scheme - 2 : Three Dimensional Parity (3DP)
• Scheme - 3 : Dynamic Dual Grain Sparing (DDS)
• Summary
WHY SPARE FAULTY DATA?

• Correcting Large Faults Has Performance Overhead

• To prevent accumulation of faults

Sparing Mitigates Performance Overheads and Enhances Reliability
TRACKING STRUCTURES IN SPARING

• Row Level Tracking
  – Large Indirection Structure
  – Sparing Area Used Efficiently

• Bank Level Tracking
  – Small Indirection Structure
  – Sparing Area Used Inefficiently

Ideally We Need Small Indirection Structures Which Use Spare Area Efficiently
• Observation: Either < 4 or > 4000 row failures

66.8% Affecting less than 4 rows
33.2% Affecting more than 4000 rows

Number of Faulty Rows in a Faulty Bank

Spare Faulty Regions At Two Granularities
Dynamic Dual Grain Sparing

- Provision Spare Area for Two Granularities

- Use a spare bank
- Use an entire spare row

Dual Grain Sparing Efficiently Uses Spare Area
Citadel provides **700X** more resilience, consuming only 4% additional power and 1% additional execution time.

System: 8GB HBM @ DDR3-1600
Baseline: No Protection + Same Bank

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Slowdown</th>
<th>Active Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>ChipKill</td>
<td>1.25</td>
<td>3.8X</td>
</tr>
<tr>
<td>Citadel</td>
<td>1.01</td>
<td>1.04X</td>
</tr>
</tbody>
</table>
• Introduction and Background
• Citadel
• Scheme - 1 : TSV-SWAP
• Scheme - 2 : Three Dimensional Parity (3DP)
• Scheme - 3 : Dynamic Dual Grain Sparing (DDS)
• Summary
SUMMARY

• 3D stacking can enable high bandwidth DRAM
• Newer failure modes like TSV failures
• Striping data to protect against faults is costly
• Citadel enables robust and efficient 3D DRAM by:
  – TSV-SWAP runtime TSV SPARING
  – Handling multiple-faults using 3DP
  – Isolating faults using DDS
• Citadel provides all benefits of stacking at 700X higher resilience without the need for striping data
Thank You

Questions?
BACKUP SLIDES
Recent papers** shows that

1. TSVs prone to EM-induced voiding effects**
2. Interfacial cracks → thermal-mechanical stress**
3. EM-induced voids increase TSV resistance, causing path delay faults and TSV open defects**
4. Micro-Bump faults+

*Li Jiang et. al. [DAC 2013]
+Krishnendu C. et. al. [IRPS 2012]
TSV-SWAP REPAIR CIRCUIT

Data TSV-Lane

Enable TSV-SWAP

Standby TSV

Standby-TSV Lane

Pass Transistors

TSV REDIR REG (TRR)

0

-----

1

1

TSV-0

Lane

----

TSV-0

TSV-m

TSV-m

(Connect Standby TSV, Enable TSV-SWAP=1)
PARITY CACHE: HIT RATE

Benchmarks

Percentage Hit Rate

SPEC FP  SPEC INT  PARSEC  BIOBENCH  GMEAN